GATE ETCH PROCESS FOR A HIGH-VOLTAGE FET

This application is a continuation of application Ser. No. 11/542,083, filed Oct. 3, 2006, entitled, "Gate Etch Process for a High-Voltage FET", which is assigned to the assignee of the present application.

TECHNICAL FIELD

The present disclosure relates to semiconductor processes for fabricating high-voltage, field-effect transistors.

BACKGROUND

High-voltage, field-effect transistors (HVFETs) are well known in the semiconductor arts. Many HVFETs employ a device structure that includes an extended drain region that supports or blocks the applied high-voltage (e.g., several hundred volts) when the device is in the "off" state. In a conventional vertical HVFET structure, a mesa of semiconductor material forms the extended drain or drift region for current flow in the on-state. A trench gate structure is formed near the top of the substrate, adjacent the sidewall regions of the mesa where the body region is disposed. Application of an appropriate voltage potential to the gate causes a conductive channel to be formed along the vertical sidewall portion of the body region such that current may flow vertically through the semiconductor material, i.e., from a top surface of the substrate where the source region is disposed, down to the bottom of the substrate where the drain region is located.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example, and not limitation, in the figures of the accompanying drawings, wherein:

FIG. **1**A illustrates an example cross-sectional side view of a vertical HVFET in a fabrication process after the initial step of forming an epitaxial layer on a substrate.

FIG. **1**B illustrates the example device structure of FIG. **1**A following vertical trench etching that forms a silicon mesa.

FIG. **1**C illustrates the example device structure of FIG. **1**B after formation of a dielectric layer on the sidewalls of the mesa and filling of the remaining portions of the trenches with polysilicon.

FIG. **1**D illustrates the example device structure of FIG. **1**C after masking of a top surface of the silicon substrate.

FIG. **1**E illustrates the example device structure of FIG. **1**D after formation of the gate trenches.

FIG. **1**F illustrates the example device structure of FIG. **1**E following removal of the oxide covering the sidewalls of the mesa in the gate trenches.

FIG. **1**G illustrates the example device structure of FIG. **1**F after removal of the masking layer, formation of a thin gate oxide the sidewalls of the mesa, and subsequent filling of the gate trenches.

FIG. **1**H illustrates the example device structure of FIG. **1**G in an expanded view that shows the field plates in relation to the trench gate structure.

FIG. **1**I illustrates the example device structure of FIG. **1**H after formation of the source and body regions.

DESCRIPTION OF EXAMPLE EMBODIMENTS

In the following description specific details are set forth, such as material types, dimensions, structural features, processing steps, etc., in order to provide a thorough understanding of the present invention. However, persons having ordinary skill in the relevant arts will appreciate that these specific details may not be needed to practice the present invention.

It should be understood that the elements in the figures are representational, and are not drawn to scale in the interest of clarity. It is also appreciated that although a method for fabricating an N-channel HVFET device is disclosed, a P-channel HVFET may also be fabricated by utilizing the opposite conductivity types for all of the illustrated doped regions. Furthermore, although the figures appear to show a single device, those of skill will understand that such transistor structures are commonly fabricated in a repeated, inter-digitated, or otherwise replicated manner. In other words, the method for fabricating a vertical HVFET device structure shown by way of the various example processing steps in FIGS. **1**A-**1**I may be utilized to construct a device having plurality of parallel-arranged or replicated regions.

FIG. **1** illustrates an example cross-sectional side view of a vertical HVFET in a fabrication process after the initial step of forming an epitaxial layer **12** of N-type semiconductor material on an N+ doped silicon substrate **11**. In one embodiment, epitaxial layer **12** has a vertical thickness in a range about 15 μm to 120 μm thick. The N+ substrate **11** is heavily doped to minimize its resistance to current flowing through to the drain electrode, which is located on the bottom of the substrate in the completed device. Doping of epitaxial layer **12** may be carried out as the layer is being formed. In one embodiment, the doping concentration of epitaxial layer **12** is linearly graded to produce an extended drain region that exhibits a substantially uniform electric-field distribution. Linear grading may stop at some point below the top surface of the epitaxial layer **12**.

After epitaxial layer **12** has been formed, the top surface of the semiconductor wafer is appropriately masked and deep vertical trenches are then etched into epitaxial layer **12**. FIG. **1**B illustrates an example cross-sectional side view of a vertical HVFET in a fabrication process following vertical trench etching that forms a silicon mesa **14**. The height and width of mesa **14**, as well as the spacing between adjacent vertical trenches may be determined by the breakdown voltage requirements of the device. Mesa **14** of epitaxial material **12** eventually forms the N-type drift region of the final HVFET device structure. It should be understood that mesa **14**, in various embodiments, may extend a considerable lateral distance in an orthogonal direction (into and out of the page). In certain embodiments, the lateral width of the N-type drift region formed by mesa **14** is as narrow as can be reliably manufactured in order to achieve a very high breakdown voltage (e.g., 600V).

FIG. **1**C illustrates the example device structure of FIG. **1**B after formation of a dielectric layer, on the sidewalls of mesa **14** to form oxide regions **15**, and subsequent filling of the remaining portions of the trenches with polysilicon or another suitable material to form field plates **35***a* & **35***b*. The dielectric layer preferably comprises silicon dioxide, though silicon nitride or other suitable dielectric materials may also be used. In this example, oxide region **15***a* covers sidewall **19***a* of mesa **14**, while oxide region **15***b* covers sidewall **19***b* on the opposite side of mesa **14**. Sidewall oxide regions **15***a* & **15***b* also cover the exposed portion of N+ substrate **11** in each of the respective trenches. Oxide regions **15** may be formed using a variety of well-known methods, including thermal growth and chemical vapor deposition.

Following the formation of sidewall oxide regions **15**, the remaining open portions of the trenches are filled with a conductive material that forms field plates **35***a* & **35***b*. The top